7. (Once Amended) A method for etching a feature [with minimal RIE lag] in an integrated circuit wafer, the method comprising:

positioning the wafer in a reaction chamber;

etching through a first layer of organosilicate glass dielectric, comprising:

providing a flow of an etchant gas mixture including C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

STATEMENT OF COMMON OWNERSHIP

At the time this invention was made, this invention as claimed in this application and Marquez (U.S. Patent 6,228,774) were both owned by, or subject to an obligation of assignment to Lam Research Corporation.

REMARKS

Claims 1 and 7 have been amended.

The election of Group I, claims 1-14 is affirmed.

The Examiner rejected claims 1-5 and 7-10 under 35 U.S.C. 103(a) as being unpatentable over Marquez (US 6,228,774 B1) in view of Wolf et al. Marquez combined with Wolf would not make obvious introducing a flow of etchant gas including C4F8 and CF4 into a reaction chamber to etch an organosilicate glass dielectric as recited in claims 1 and 7. Marquez cites an etchant gas with C4F8 and Wolf recites CF4. The Examiner stated that Wolf discloses the use of CF4 on page 550 to move the C/F ratio to provide a higher etch rate to an optimized F/C ratio described on page 551. The optimized etch ratio described on page 551 of Wolf is the "value close to that which exists in pure CF4." If that is the F/C ratio taught in Wolf, then it would not be obvious to combine C4F8 with CF4, since the C4F8 would move the F/C ratio away from the desired ratio taught in Wolf. In addition, Marquez is an improper 103 reference, since Marquez and the present invention are commonly owned, as stated above, and since the present invention was filed before Marquez issued. For at least these reasons, claims 1 and 7 are not made obvious by Marquez in view of Wolf.

Claims 2-6 and 8-14 are ultimately dependent on claims 1 or 7, and are therefore respectfully submitted to be patentable over the art of record for at least the reasons set forth above with respect to claims 1 and 7. Additionally, these dependent claims require additional elements that, when taken in the context of the claimed invention, further patentably distinguish the art of record. For example, claim 2 recites the addition of CH2F2. For at least these reasons, claims 2-5 and 8-10 are not made obvious by the cited references.

The Examiner rejected claims 1-14 under 35 U.S.C. 112, second paragraph, as being indefinite. The Examiner stated that "minimal RIE lag" is indefinite. The phrase "minimal RIE lag" has been deleted accordingly.

In view of the amendments set forth above, it is respectfully submitted that the application is in a condition for allowance and action to that effect is respectfully requested at an early date. If the Examiner feels that a telephone conference would expedite allowance of this application, the Examiner is invited to call the undersigned at (831) 655-2300.

The Commissioner is authorized to charge any fees that may be due to our Deposit Account No. 50-0388 (LAM1P154).

Respectfully submitted,

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CLEAN VERSION OF PENDING CLAIMS

1. (Once Amended) A method for etching a feature in an integrated circuit wafer incorporating at least one layer of organosilicate glass dielectric, the method comprising:

positioning the wafer in a reaction chamber;

introducing a flow of etchant gas mixture including C4F8 and CF4 into the reaction chamber; and

striking a plasma with the etchant gas in the reaction chamber.

2. The method, as recited in claim 1, wherein the etchant gas mixture further comprises CH2F2.

3. The method, as recited in claim 2, wherein the etchant gas mixture further comprises oxygen.

4. The method, as recited in claim 3, wherein the etchant gas mixture further comprises argon.

5. The method, as recited in claim 4, further comprising etching a first layer of organosilicate glass dielectric with the plasma from the etchant gas comprising C4F8, CF4, CH2F2, oxygen and argon.

6. The method, as recited in claim 5, further comprising stopping the flow of CH2F2 and C4F8 in the etchant gas and using the resulting plasma to etch through an etch stop layer.

7. (Once Amended) A method for etching a feature in an integrated circuit wafer, the method comprising:

positioning the wafer in a reaction chamber;

etching through a first layer of organosilicate glass dielectric, comprising:

providing a flow of an etchant gas mixture including C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

8. The method, as recited in claim 7, wherein the etchant gas mixture for etching through the first layer of organosilicate glass, further comprises CH2F2.

9. The method, as recited in claim 8, wherein the etchant gas mixture for etching through the first layer of organosilicate glass, further comprises oxygen.

10. The method, as recited in claim 9, wherein the etchant gas mixture for etching through the first layer of organosilicate glass, further comprises argon.

11. The method, as recited in claim 10, further comprising etching through an etch stop layer, comprising:

providing an etchant gas mixture without C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

12. The method, as recited in claim 10, further comprising etching through an etch stop layer after etching through the first layer of organosilicate glass, comprising:

stopping the flow of C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

13. The method, as recited in claim 12, further comprising etching through a second layer of organosilicate glass dielectric, comprising:

restarting the flow of C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

14. The method, as recited in claim 13, further comprising stripping a photoresist mask, comprising:

stopping the flow of C4F8 and CF4 into the reaction chamber;

providing a flow of nitrogen into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

15. An integrated circuit formed by the method comprising:

positioning a wafer in a reaction chamber;

etching through a first layer of organosilicate glass dielectric over the wafer, comprising:

providing a flow of an etchant gas mixture including C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

16. The integrated circuit, as recited in claim 15, wherein the etchant gas mixture for etching through the first layer of organosilicate glass, further comprises CH2F2, oxygen, and argon.

17. The integrated circuit, as recited in claim 16, wherein the method further comprises etching through an etch stop layer, comprising:

providing an etchant gas mixture without C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.

18. The integrated circuit, as recited in claim 16, wherein the method further comprises etching through an etch stop layer after etching through the first layer of organosilicate glass, comprising:

stopping the flow of C4F8 and CF4 into the reaction chamber; and

generating a plasma with the resulting etchant gas in the reaction chamber.

19. The integrated circuit, as recited in claim 18, wherein the method further comprises etching through a second layer of organosilicate glass dielectric, comprising:

restarting the flow of C4F8 and CF4 into the reaction chamber; and

generating a plasma with the etchant gas in the reaction chamber.